ABSTRACT

Process of fabricating multi-bit charge trapping dielectric flash memory device, including forming on a semiconductor substrate a bottom oxide layer to define a substrate/oxide interface, in which the bottom oxide layer includes a first oxygen concentration and a first nitrogen concentration; and adding a quantity of nitrogen to the bottom oxide layer, whereby the bottom oxide layer includes a first region adjacent the charge storage layer and a second region adjacent the substrate/oxide interface, the second region having a second oxygen concentration and a second nitrogen concentration, in which the second nitrogen concentration exceeds the first nitrogen concentration, provided that the second nitrogen concentration does not exceed the second oxygen concentration. In one embodiment, the first nitrogen concentration is substantially zero.